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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/552,076	10/04/2005	Andrei Terechko	NL 030344	8796

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PHILIPS INTELLECTUAL PROPERTY & STANDARDS
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EXAMINER	
VICARY, KEITH E	

ART UNIT	PAPER NUMBER
2196	

DATE MAILED: 12/15/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/552,076	TERECHKO, ANDREI	
	Examiner	Art Unit	
	Keith Vicary	2196	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/04/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-5 are pending for examination in this office action.

Specification

2. The following guidelines illustrate the preferred layout for the specification of a utility application. These guidelines are suggested for the applicant's use.

Arrangement of the Specification

As provided in 37 CFR 1.77(b), the specification of a utility application should include the following sections in order. Each of the lettered items should appear in upper case, without underlining or bold type, as a section heading. If no text follows the section heading, the phrase "Not Applicable" should follow the section heading:

(a) TITLE OF THE INVENTION.
(b) CROSS-REFERENCE TO RELATED APPLICATIONS.
(c) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT.
(d) THE NAMES OF THE PARTIES TO A JOINT RESEARCH AGREEMENT.
(e) INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC.
(f) BACKGROUND OF THE INVENTION.
    (1) Field of the Invention.
    (2) Description of Related Art including information disclosed under 37 CFR 1.97 and 1.98.
(g) BRIEF SUMMARY OF THE INVENTION.
(h) BRIEF DESCRIPTION OF THE SEVERAL VIEWS OF THE DRAWING(S).
(i) DETAILED DESCRIPTION OF THE INVENTION.
(j) CLAIM OR CLAIMS (commencing on a separate sheet).
(k) ABSTRACT OF THE DISCLOSURE (commencing on a separate sheet).
(l) SEQUENCE LISTING (See MPEP § 2424 and 37 CFR 1.821-1.825. A "Sequence Listing" is required on paper if the application discloses a nucleotide or amino acid sequence as defined in 37 CFR 1.821(a) and if the required "Sequence Listing" is not submitted as an electronic document on compact disc).

3. The specification is objected to for not having the section headings of background of the invention, brief summary of the invention, brief description of the several views of the drawings, and detailed description of the invention. Appropriate correction is required.

Claim Objections

4. Claim 5 is objected to because of the following informalities:

a. In claim 5, line 7, "additional additional" should be "additional."

Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 3, and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Batten et al. (Batten) (US 6269437) in view of Nickolls et al. (Nickolls) (US 5598408).

Consider claim 1, Batten discloses a clustered Instruction Level Parallelism processor (col. 7, lines 4-7 and col. 11, lines 1-4), comprising a plurality of clusters (A - D) each comprising at least one register file and at least one functional unit (col. 1; lines 43-45); an instruction unit (IFD) for issuing control signals to said clusters (A - D) (col. 11, lines 3-4; the control signals are inherent in D-H of Figure 12 and col. 11, line 65), wherein said instruction unit (IFD) is

connected to each of said clusters (A - D) via respective control connections (CA - CD) (col. 11, lines 3-4; D-H of Figure 12 and col. 11, line 65).

However, Batten does not disclose that one or more additional pipeline register (P) is arranged in said control connections (CA - CD) depending on the distance between said instruction unit (IFD) and said clusters (A - D).

On the other hand, Nickolls does disclose that one or more additional pipeline register (P) is arranged in said control connections (CA - CD) depending on the distance between said instruction unit (IFD) and said clusters (A - D) (col. 6, lines 1-45, col. 7, lines 55-60, col. 21, lines 13-32, col. 22, lines 30-42 and 56-62, col. 23, lines 13-16, col. 59, lines 64-67, col. 60, lines 1-6).

Adding in pipeline registers to serve as intermediate points for signals allows for more flexibility in component density, allows for instruction synchronization, allows for greater overall improvements in performance by adding additional clusters/processors, and increases throughput of said signals (Nickolls, col. 2, lines 30-36; col. 2, lines 54-57; col. 2, lines 60-64; col. 3, lines 55-64; col. 4, lines 1-14; col. 5, lines 51-64; col. 20, lines 11-31; col. 23, lines 13-16). Furthermore, the invention of Nickolls fits into the environment of Batten as both are sending message bits/signals to destination processors/clusters.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the invention of Batten with the pipeline registers of Nickolls in order to allow for more flexibility in component density, allow for instruction synchronization, allow for greater overall improvements in

performance by adding additional clusters/processors, and increase throughput of said signals.

Consider claim 5, Batten discloses a clustered Instruction Level Parallelism processor (col. 7, lines 4-7 and col. 11, lines 1-4), comprising: a plurality of clusters (A - D) each comprising at least one register file and at least one functional unit (col. 1, lines 43-45); an instruction unit (IFD) for issuing control signals to said clusters (A - D) (col. 11, lines 3-4; the control signals are inherent in D-H of Figure 12 and col. 11, line 65), wherein said instruction unit (IFD) is connected to each of said clusters (A - D) via respective control connections (CA - CD) (col. 11, lines 3-4; D-H of Figure 12 and col. 11, line 65).

However, Batten does not disclose that one or more additional pipeline register (P) is arranged in said control connections (CA - CD) depending on the distance between said instruction unit (IFD) and clusters (A - D).

On the other hand, Nickolls does disclose that one or more additional pipeline register (P) is arranged in said control connections (CA - CD) depending on the distance between said instruction unit (IFD) and clusters (A - D) (col. 6, lines 1-45, col. 7, lines 55-60, col. 21, lines 13-32, col. 22, lines 30-42 and 56-62, col. 23, lines 13-16, col. 59, lines 64-67, col. 60, lines 1-6).

Adding in pipeline registers to serve as intermediate points for signals allows for more flexibility in component density, allows for instruction synchronization, allows for greater overall improvements in performance by

adding additional clusters/processors, and increases throughput of said signals (Nickolls, col. 2, lines 30-36; col. 2, lines 54-57; col. 2, lines 60-64; col. 3, lines 55-64; col. 4, lines 1-14; col. 5, lines 51-64; col. 20, lines 11-31; col. 23, lines 13-16). Furthermore, the invention of Nickolls fits into the environment of Batten as both are sending message bits/signals to destination processors/clusters.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the invention of Batten with the pipeline registers of Nickolls in order to allow for more flexibility in component density, allow for instruction synchronization, allow for greater overall improvements in performance by adding additional clusters/processors, and increase throughput of said signals.

Consider claim 3, Batten discloses that said clusters (A – D) are connected to each other via a bus connection (100) (col. 9, line 66).

7. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Batten and Nickolls as applied to claim 1 above, and further in view of Parcerisa et al. (Parcerisa) (Efficient Interconnects).

Consider claim 2, although Batten discloses that any suitable structure may be used (col. 9, lines 63-66), Batten and Nickolls nevertheless do not explicitly disclose that said clusters (A – D) are connected to each other via a point-to-point connection.

On the other hand, Parcerisa does disclose that said clusters (A – D) are connected to each other via a point-to-point connection (Section 3.5, second paragraph). Furthermore, it is noted that a point-to-point interconnection structure is very well-known in many arts as a method for interconnection.

The motivation to use a point-to-point interconnection structure results in shorter delays, a lower network cost, and better scalability than a bus-based interconnection structure (Parcerisa, Section 3.5, second paragraph). The disclosed point-to-point interconnection fits into the environment of the invention of Batten and Nickolls because both deal with interconnections for clustered microarchitectures.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Parcerisa with the invention of Batten and Nickolls in order to have shorter delays, a lower network cost, and better scalability.

8. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Batten and Nickolls as applied to claim 3 above, and further in view of Pechanek et al. (Pechanek) (US PAT 5659785).

Consider claim 4, Batten and Nickolls do not explicitly disclose that said control connections (CA – CD) are implemented as a bus (110).

On the other hand, Pechanek does disclose that said control connections (CA – CD) are implemented as a bus (110) (col. 5, lines 33-39; each PE is

analogous to each cluster and each SP is analogous to the IFD from which the control connections emanate). Furthermore, it is noted that the use of a bus to carry signals from a central source to multiple destinations is very well-known in the art.

Using a bus to carry control connections is advantageous because the wiring is easily implemented, and results in a reduction of mass and costs. The disclosed bus of Pechanek also fits into the environment of Batten and Nickolls as both are related to communication architectures between a control unit and its corresponding clusters/processor elements.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teaching of Pechanek with the invention of Batten and Nickolls in order to result in easy wiring implementation and a reduction of mass and costs.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Keith Vicary whose telephone number is (571) 270-1314. The examiner can normally be reached on Monday - Friday, 8:00 a.m. - 5:00 p.m., EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nabil El-Hady can be reached on 571-272-3963. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

KV
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SUPERVISORY PATENT EXAMINER